IN THE CLAIMS:

Claims 40 through 55 were previously cancelled. None of the claims have been amended herein. All of the pending claims are presented below for convenience of the Examiner. Please enter these claims as previously amended.

1. (Previously presented) An integrated circuit device comprising:

a first conductive layer including at least one protrusion;

an insulative layer overlying the first conductive layer and exposing at least part of the at least one protrusion; and

a programmable resistive material overlying directly above at least part of the insulative layer and in direct contact with the at least one protrusion of the first conductive layer, the programmable resistive material capable of switching between different resistive states.

2. (Previously presented) The integrated circuit device of claim 1, wherein the programmable resistive material is formulated to be reversibly cycled between at least two different resistive states.

3. (Previously presented) The integrated circuit device of claim 1, wherein the exposed part of the at least one protrusion comprises a smaller cross-sectional area than a remaining part of the at least one protrusion of the first conductive layer.

4. (Previously presented) The integrated circuit device of claim 1, wherein the programmable resistive material comprises a chalcogenide material.

5. (Previously presented) The integrated circuit device of claim 4, wherein the chalcogenide material is selected from a group consisting of tellurium (Te), germanium (Ge), antimony (Sb), and combinations thereof.

6. (Previously presented) The integrated circuit device of claim 4, wherein the chalcogenide material includes tellurium (Te), germanium (Ge), and antimony (Sb) in a ratio of $Te_aGe_bSb_{100-(a+b)}$, where a, b, and 100-(a+b) are in atomic percentages which total 100% of the constituent elements and $a \leq 70$ and $15 \leq b \leq 50$.

7. (Original) The integrated circuit device of claim 6, wherein $40 \leq a \leq 60$ and $17 \leq b \leq 44$.

8. (Previously presented) The integrated circuit device of claim 1, further comprising a second conductive layer above the programmable resistive material.

9. (Previously presented) The integrated circuit device of claim 8, wherein the second conductive layer comprises titanium nitride or carbon.

10. (Previously presented) The integrated circuit device of claim 8, further comprising a conductive barrier layer between the programmable resistive material and the second conductive layer.

11. (Previously presented) The integrated circuit device of claim 1, further comprising a second conductive layer in direct contact with the programmable resistive material.

12. (Previously presented) The integrated circuit device of claim 1, further comprising a second conductive layer above the programmable resistive material and an interlayer dielectric over the second conductive layer, the interlayer dielectric including an aperture that exposes at least a portion of an upper surface of the second conductive layer.

13. (Previously presented) The integrated circuit device of claim 12, further comprising a conductive grid interconnect within the aperture.

14. (Previously presented) The integrated circuit device of claim 13, wherein the conductive grid interconnect is selected from the group consisting of titanium, titanium nitride and aluminum.

15. (Previously presented) The integrated circuit device of claim 1, wherein a portion of the at least one protrusion comprises a frustoconical tip.

16. (Previously presented) The integrated circuit device of claim 15, wherein the frustoconical tip has a frustum lateral dimension of at least 0.1 μm.

17. (Previously presented) The integrated circuit device of claim 15, wherein the frustoconical tip has a frustum lateral dimension of about 0.4 μm.

18. (Previously presented) The integrated circuit device of claim 15, wherein the frustoconical tip has a height of approximately 2000 Å.

19. (Previously presented) The integrated circuit device of claim 1, further comprising an opening through the insulative layer such that the at least part of the first conductive layer is exposed.

20. (Previously presented) The integrated circuit device of claim 19, wherein the programmable resistive material is at least within the opening.

21. (Previously presented) An integrated circuit device comprising:

a first electrode having a first portion and a second portion, a width of the first electrode narrowing substantially and continuously in a direction extending from the second portion toward the first portion of the first electrode;

an insulative layer proximate the first electrode;

a layer of programmable resistive material in contact with the first portion of the first electrode and overlying directly above at least part of the insulative layer, the programmable resistive material capable of being reversibly cycled; and

a second electrode coupled to the layer of programmable resistive material.

22. (Previously presented) The integrated circuit device of claim 21, wherein the programmable resistive material is formulated to be reversibly cycled between at least two different resistive states.

23. (Previously presented) The integrated circuit device of claim 21, wherein the programmable resistive material comprises a chalcogenide material.

24. (Previously presented) The integrated circuit device of claim 23, wherein the chalcogenide material is selected from a group consisting of tellurium (Te), germanium (Ge), antimony (Sb), and combinations thereof.

25. (Previously presented) The integrated circuit device of claim 23, wherein the chalcogenide material includes tellurium (Te), germanium (Ge), and antimony (Sb) in a ratio of $Te_aGe_bSb_{100-(a+b)}$, where a, b, and 100-(a+b) are in atomic percentages which total 100% of the constituent elements and $a \leq 70$ and $15 \leq b \leq 50$.

26. (Original) The integrated circuit device of claim 25, wherein $40 \leq a \leq 60$ and $17 \leq b \leq 44$.

27. (Previously presented) The integrated circuit device of claim 21, wherein the second electrode comprises titanium nitride or carbon.

28. (Previously presented) The integrated circuit device of claim 21, further comprising a conductive barrier layer between the programmable resistive material and the second electrode.

29. (Previously presented) The integrated circuit device of claim 21, wherein the second electrode is in direct contact with the programmable resistive material.

30. (Previously presented) The integrated circuit device of claim 21, further comprising an interlayer dielectric over the second electrode, the interlayer dielectric including an aperture that exposes at least a portion of an upper surface of the second electrode.

31. (Previously presented) The integrated circuit device of claim 30, further comprising a conductive grid interconnect within the aperture.

32. (Previously presented) The integrated circuit device of claim 31, wherein the conductive grid interconnect is selected from the group consisting of titanium, titanium nitride and aluminum.

33. (Previously presented) The integrated circuit device of claim 21, wherein the first portion of the first electrode comprises a frustoconical tip.

34. (Previously presented) The integrated circuit device of claim 33, wherein the frustoconical tip has a frustum lateral dimension of at least 0.1 μm.

35. (Previously presented) The integrated circuit device of claim 34, wherein the frustoconical tip has a frustum lateral dimension of about 0.4 μm.

36. (Previously presented) The integrated circuit device of claim 33, wherein the frustoconical tip has a height of approximately 2000 Å.

37. (Previously presented) The integrated circuit device of claim 21, further comprising an insulative layer above the first electrode.

38. (Previously presented) The integrated circuit device of claim 37, further comprising an opening through the insulative layer such that at least part of the first portion of the first electrode is exposed.

39. (Previously presented) The integrated circuit device of claim 38, wherein the programmable resistive material is at least within the opening.

40.-55. (Cancelled)

56. (Previously presented) A semiconductor memory cell comprising:

a first conductive layer on a substrate, wherein the first conductive layer includes at least one raised portion;

an insulative layer proximate the at least one raised portion;

a programmable resistive material in direct contact with the at least one raised portion of the first conductive layer and overlying directly above at least part of the insulative layer, the programmable resistive material configured to switch between different resistive states; and

a second conductive layer above the programmable resistive material.

57. (Previously presented) The semiconductor memory cell of claim 56, wherein the programmable resistive material comprises a chalcogenide material.

58. (Previously presented) The semiconductor memory cell of claim 57, wherein the chalcogenide material is selected from a group consisting of tellurium (Te), germanium (Ge), antimony (Sb), and combinations thereof.

59. (Previously presented) The semiconductor memory cell of claim 57, wherein the chalcogenide material includes tellurium (Te), germanium (Ge), and antimony (Sb) in a ratio of $Te_aGe_bSb_{100-(a+b)}$, where a, b, and 100-(a+b) are in atomic percentages which total 100% of the constituent elements and $a \leq 70$ and $15 \leq b \leq 50$.

60. (Original) The semiconductor memory cell of claim 59, wherein $40 \leq a \leq 60$ and $17 \leq b \leq 44$.

61. (Previously presented) The semiconductor memory cell of claim 56, further comprising a conductive barrier layer between the programmable resistive material and the second conductive layer.

62. (Previously presented) The semiconductor memory cell of claim 56, wherein the second conductive layer is in direct contact with the programmable resistive material.

63. (Previously presented) The semiconductor memory cell of claim 56, further comprising an interlayer dielectric over the second conductive layer, the interlayer dielectric including an aperture that exposes at least a portion of an upper surface of the second conductive layer.

64. (Previously presented) The semiconductor memory cell of claim 63, further comprising a conductive grid interconnect within the aperture.

65. (Previously presented) The semiconductor memory cell of claim 64, wherein the conductive grid interconnect is selected from the group consisting of titanium, titanium nitride and aluminum.

66. (Previously presented) The semiconductor memory cell of claim 56, wherein a portion of the at least one raised portion comprises a frustoconical tip.

67. (Previously presented) The semiconductor memory cell of claim 66, wherein the frustoconical tip has a frustum lateral dimension of at least 0.1 μm.

68. (Previously presented) The semiconductor memory cell of claim 66, wherein the frustoconical tip has a frustum lateral dimension of about 0.4 μm.

69. (Previously presented) The semiconductor memory cell of claim 66, wherein the frustoconical tip has a height of approximately 2000 Å.

70. (Previously presented) The semiconductor memory cell of claim 56, wherein the second conductive layer comprises titanium nitride or carbon.

71. (Previously presented) The semiconductor memory cell of claim 56, further comprising an insulative material over the first conductive layer and having an opening therethrough such that at least a portion of the first conductive layer is exposed.

72. (Previously presented) The semiconductor memory cell of claim 71, wherein the programmable resistive material is at least within the opening.